DW 2183

PTO/SB/21 (09-04)

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/838,678
Filing Date	April 19, 2001
First Named Inventor	Uht, Augustus K.
Art Unit	2183
Examiner Name	O'BRIEN, BARRY J.
Total Number of Pages in This Submission: 12	Attorney Docket Number: 022193-010310US

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☒ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
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- ☐ Drawing(s)
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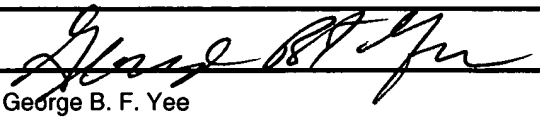
Signature			
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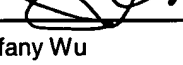
Signature			
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PATENT
Attorney Docket No.: 022193-010310US
Client Reference No.: URI-165

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Augustus K. Uht et al.

Application No.: 09/838,678

Filed: April 19, 2001

For: AUTOMATIC AND TRANSPARENT HARDWARE CONVERSION OF TRADITIONAL CONTROL FLOW TO PREDICATES

Examiner: O'BRIEN, BARRY J.

Art Unit: 2183

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97 and §1.98

Commissioner for Patents
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Alexandria, VA 22313-1450

Sir:

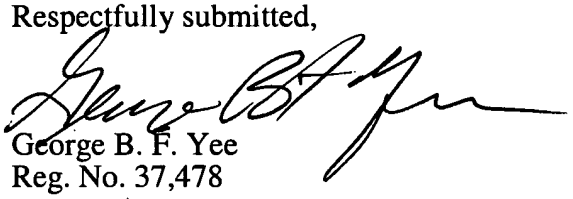
The references cited on attached form PTO/SB/08A and PTO/SB/08B are being called to the attention of the Examiner. Copies of the references are enclosed. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no

representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

Applicant believes that no fee is required for submission of this statement. However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,



George B. F. Yee
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PTO/SB/08A (08-03)

Substitute for Form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 8

Complete if Known	
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Art Unit	2183
Examiner Name	O'BRIEN, BARRY J.
Attorney Docket Number	022193-010310US

U.S. PATENT DOCUMENTS+

Examiner Initials*	Cite No.[1]	Document Number: Number Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 2 of 8

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NON PATENT LITERATURE DOCUMENTS

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	1	Agerwala et al., "Data Flow Systems - Special Issue," *IEEE COMPUTER,* vol. 15, no. 2, pp. 10-13,1982.	
	2	Aiken et al., "Perfect Pipelining: A New Loop Parallelization Technique," in *Proceedings of the* 1988 *European Symposium on Programming,* 1988, 15 pages total.	
	3	Austin et al., "Dynamic Dependency Analysis of Ordinary Programs," in *Proceedings of the 19th Annual International Symposium on Computer Architecture, Gold Coast, Australia,* pp. 342-351, IEEE and ACM, May 1992	
	4	Banerjee et al., "Fast Execution of Loops With IF Statements," *IEEE Transactions on Computers,* vol. C-33, pp. 1030-1033, November 1984.	
	5	Beck et al., "The cydra 5 minisupercomputer: Architecture and implementation," *Journal of Supercomputing,* vol. 7, pp. 143-180, 1993.	
	6	Brekelbaum et al., "Hierarchical Scheduling Windows," in *Proceedings of the 35th Annual International Symposium on Microarchitecture.* Istanbul, Turkey: IEEE, ACM, November 2002.	
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	10	Chen, "Supporting Highly Speculative Execution via Adaptive Branch Trees," in *Proceedings of the 4th Annual International Symposium on High Peiformance Computer Architecture:* IEEE, January 1998, pp. 185-194.	
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	12	Cleary et al., "The Architecture or an Optimistic CPU: The Warp Engine," in *Proceedings of the HICSS'95,* pp.163-172, University of Hawaii, January 1995.	
	13	Colwell et al., "A VLIW Architecture For A Trace Scheduling Compiler," *IEEE Transactions on Computers,* vol. C-37, pp. 967-979, August 1988.	
	14	Colwell et al., "A VLIW Architecture for a Trace Scheduling Compiler," in *Proceedings of the Second International Conference Architectural Support for Programming Languages and Operating Systems (ASP LOS II):* ACM and IEEE, September 1987, pp. 180-192.	
	15	Cragon, *Branch Strategy Taxonomy and Performance Models,* Los Alamitos, California: IEEE Computer Society Press, 1992, 9 pages total.	
	16	Cytron, "Doacross: Beyond Vectorization for Multiprocessors (Extended Abstract)," in *Proceedings of the* 1986 *International Conference on Parallel Processing,* pp. 836-844, Pennsylvania State University and the IEEE Computer Society, August 1986.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				*Application Number*	09/838,678
				Filing Date	April 19, 2001
				First Named Inventor	Uht, Augustus K.
				Art Unit	2183
(use as many sheets as necessary)				*Examiner Name*	O'BRIEN, BARRY J.
Sheet	3	of	8	*Attorney Docket Number*	022193-010310US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	17	Dutta et al., "Control Flow Prediction with Tree-Like Subgraphs for Superscalar Processors," in *Proceedings of the 28th International Symposium on Micmarchitecture (MICRO-28),* pp. 258-263, IEEE and ACM, November/December 1995.	
	18	Ebcioglu et al., "DAISY: Dynamic Compilation for 100% Architectural Compatibility," IBM Research Report RC 20538, IBM Research Division, August 5, 1996, 82 pages total.	
	19	Ebcioglu, "A Compilation Technique for Software Pipelining of Loops with Conditional Jumps," in *Proceedings of the Twentieth Annual Workshop on Microprogramming (MICRO20),* pp. 69-79, Association of Computing Machinery, December 1987	
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	27	Gopal et al., "Speculative Versioning Cache," University of Wisconsin, Madison, Technical Report TR-1334, 11 pages total, July 1997.	
	28	Gostelow, "The u-interpreter," *IEEE Computer,* vol. 15, pp. 42-49, February 1982.	
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	31	Henry et al., "Circuits for Wide-Window Superscalar Processors," in Proceedings of the 27th Annual International Symposium on Computer Architecture. Vancouver, BC, Canada: IEEE and ACM, June 10-14, 2000, pp. 236-247.	
	32	Henry et al., "The Ultrascalar Processor: An Asymptotically Scalable Superscalar Microarchitecture," in HIPC '98, December 1998, URL: http://ee.yale.edu/papers\HIPC98-abstract.ps.gz, 18 pages total.	

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	33	Huck et al., "Introducing the ia-64 architecture," in *IEEE Micro,* pp. 12-23, September 2000.	
	34	Jefferson, "Virtual Time," *Transactions on Programming Languages and Systems,* vol.7, no. 3, pp. 404-425, July 1985.	
	35	Jouppi et al., "Available instruction-level parallelism for superscalar and superpipelined machines," in *Proceedings of the International Conference on Architectural Suport for Programming Languages and Operating Systems,* pp. 272-282, April 1989.	
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	37	Khalafi et al., "Realizing High IPC Through a Scalable Memory-Latency Tolerant Multipath Microarchitecture," Department of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI 02881-0805, Technical Report 032002-0101, April 2, 2002, URL: http://www.ele.uri.edu/~uht/papers/Levo4TR032002-01 Ol.l)df., 11 pages total.	
	38	Kim et al., "An Instruction Set Architecture and Microarchitecture for Instruction Level Distributed Processing," in *Proceedings of the 29th Annual International Symposium on Computer Architecture.* Anchorage, Alaska, USA: ACM, May 25-29, 2002.	
	39	Klauser et al., "Dynamic Hammock Predication for Non-predicated Instruction Set Architectures," in *Intl. Conf on Parallel Architectures and Compilation Techniques (PACT).* Paris, France, October 1998, pp. 278-285.	
	40	Krewell, "IntellQ0l Earnings Plummet," *Cahners Microprocessor,* vol. 15, no. 5, May 2001, 1 page total.	
	41	Krewell, "Intel's McKinley Comes Into View," *Cahners Microprocessor,* vol. 15, no. 10, pp. 1,5 October 2001.	
	42	Kumar, "Measuring Parallelism in Computation-Intensive Scientific/Engineering Applications," *IEEE Transactions on Computers,* vol. 37, no. 9, pp. 1088-1098, September 1988.	
	43	Lam et al., "Limits of Control Flow on Parallelism," in *Proceedings of the 19th Annual International Symposium on Computer Architecture.* Gold Coast, Australia: IEEE and ACM, May 1992, pp. 46-57.	
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	45	Lee et al., "Branch Prediction Strategies and Branch Target Buffer Design," *COMPUTER,* vol. 17, pp. 6-22, January 1984.	
	46	Lepak et al., "On the value locality of store instructions," in *Proceedings of the International Symposium on Computer Architecture,* pp. 182-191, June 2000.	
	47	Lilja, "Reducing the Branch Penalty in Pipelined Processors," *COMPUTER,* vol. 21, pp. 47-55, July 1988.	

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Sheet 5 of 8

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	48	Lipasti et al., "Superspeculative Microarchitecture for Beyond AD 2000," *IEEE COMPUTER,* vol. 30, no. 9, pp. 59-66, September 1997.	
	49	Lipasti et al., "Value Locality and Load Value Prediction," in *Proceedings of the Seventh Annual International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS- VII).* Boston, MA: IEEE and ACM, October 1996, pp. 138-147.	
	50	Mahlke et al., "A Comparison of Full and Partial Predicated Execution Support for ILP Processors," in *Proceedings of the 22nd Annual International Symposium on Computer Architecture,* pp. 138-149, IEEE and ACM, May 1995.	
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	52	Morano et al., "Implications of Register and Memory Temporal Locality for Distributed Microarchitectures," Dept. of Electrical and Computer Engineering, Northeastern University, Boston, MA, USA, Technical Report, October 2002, pp 1-20, URL: http://www .ece .neu. edu/ groups/nucar/publications/interva ls. pdf	
	53	Morano et al., "Realizing High IPC Through a Scalable Memory-Latency Tolerant Multipath Microarchitecture," in *Proceedings of the Workshop On Chip Multiprocessors: Processor Architecture and Memory Hierarchy Related Issues (MEDEA 2 002), at PACT 2002.* Charlottesville, Virginia, USA, September 22, 2002, pp 16-25. Also appears in ACM SIGARCH Computer Architecture Newsletter, March 2003, URL: http://www.ele.uri.edu/~uht/papers/MEDEA2002final.pdf.	
	54	Morano, "Execution-Time Instruction Predication," Dept. of Electrical and Computer Engineering, University of Rhode Island, Kingston, RI 02881, Technical Report 0320020100, March 2002, pp. 1-10, URL: http://www.ele.uri.edu/-uht/papers/Levo3TR032002-0l00.pdf.	
	55	Nagarajan et al., "A Design Space Evaluation of Grid Processor Architectures," in *Proceedings of the 30th Annual ACM/IEEE International Symposium on Microarchitecture.* Austin, Texas, USA: ACM, December 2001, pp. 40-51.	
	56	Pajuelo et al., "Speculative Dynamic Vectorization," in *Proceedings of the 29th Annual International Symposium on Computer Architecture.* Anchorage, Alaska, USA: ACM, May 25-29, 2002.	
	57	Papworth, "Tuning the Pentium Pro Microarchitecture," *IEEE MICRO,* vol. 16, no. 2, pp. 8-15, April 1996.	
	58	Parcerisa et al., "Efficient Interconnects for Clustered Microarchitectures," in *Proceedings of the Eleventh International Conference on Parallel Architectures and Compilation Techniques.* Charlottesville, Virginia, USA: IEEE, September 22-25, 2002 10 pages total.	
	59	Park et al., "Reducing Register Ports for Higher Speed and Lower Energy," in *Proceedings of the 35th Annual International Symposium on Microarchitecture.* Istanbul, Turkey: IEEE, ACM, November 2002, 12 pages total.	
	60	Patt et al., "HPS, a New Microarchitecture: Rationale and Introduction," in *Proceedings of the Eighteenth Annual Workshop on Microprogramming (MICRO-18):* IEEE and ACM, December 1985, pp. 103-108.	
	61	Popescu et al., "The Metaflow Architecture," *IEEE MICRO,* vol. 11, no. 3, June 1991, pp. 10-13 & 63-73.	

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	62	Preston et al., "Design of an 8-wide Superscalar RISC Microprocessor with Simultaneous Multithreading," in *Proceedings of the International Solid State Circuits Conference,* January 2002. Slides from talk at conference also referenced, 6 pages total.	
	63	Raasch et al., "A Scalable Instruction Queue Using Dependence Chains," in *Proceedings of the 29th Annual International Symposium on Computer Architecture.* Anchorage, Alaska, USA: ACM, May 25-29, 2002, 12 pages total.	
	64	Rau et al., "Instruction-level parallel processing: History, overview and perspective," *International Journal of Supercomputing,* vol. 7, pp. 9-50, October 1996.	
	65	Rau et al., "The cydra 5 departmental supercomputer: Design and philosophies, decisions and tradeoffs," *IEEE Computer Magazine,* vol. 22, pp. 12-34, Jan 1989.	
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	67	Rotenberg et al., "Control independence in trace processors," in *IEEE Symposium on Microarchitecture,* pp. 4-15, December 1999.	
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	69	Sankaralingam et al., "Exploiting ILP, TLP, and DLP with the Polymorphous TRIPS Architecture," in *Proceedings of the 30th Annual International Symposium on Computer Architecture.* San Diego, California, USA: ACM and IEEE, June 9-11 2003, 12 pages total.	
	70	Sazeides et al., "The Performance Potential of Data Dependence Speculation & Collapsing," in *Proceedings of the 29th International Symposium on Microarchitecture (MICRO-29):* IEEE and ACM, December 1996, pp. 238-247.	
	71	Sazeides et al., "The predictability of data values," in *Proceedings of the 30th International Symposium on Microarchitecture,* pp. 248-258, December 1997, 11 pages total.	
	72	Seznec et al., "Register Write Specialization Register Read Specialization: A Path to Complexity-Effective Wide-Issue Superscalar Processors," in *Proceedings of the 35th Annual International Symposium on Microarchitecture.* Istanbul, Turkey: IEEE, ACM, November 2002, 12 pages total.	
	73	Smith et al., "Boosting Beyond Static Scheduling in a Superscalar Processor," in *Proceedings of the 17th Annual International Symposium on Computer Architecture,* pp. 344-354, IEEE and ACM, May 1990.	
	74	Smith, "A Study of Branch Prediction Strategies," in *Proceedings of the 8th Annual Symposium on Computer Architecture,* pp. 135-148, IEEE and ACM, 1981.	
	75	Smith, "Architecture and Applications of the HEP Multiprocessor Computer," *Society of Photo-optical Instrumentation Engineers,* no. 298, pp. 241-248, 1981.	
	76	Sohi et al., "Multiscalar processors," in *Proceedings of the International Symposium on Computer Architecture, IEEE and ACM,* pp. 414-425, June 1995.	
	77	Su et al., "GURPR - A Method for Global Software Pipelining," in *Proceedings of the Twentieth Annual Workshop on Microprogramming (MICRO-20), Association of Computing Machinery,*pp.88-96, December 1987.	

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Art Unit	2183
Examiner Name	O'BRIEN, BARRY J.
Attorney Docket Number	022193-010310US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	78	Taylor et al., "The Raw Microprocessor: A Computational Fabric for Software Circuits and General-Purpose Programs," *IEEE Micro,* vol. 22, no. 2, pp. 25-35, March-April 2002.	
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Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 8 of 8

Complete if Known	
Application Number	09/838,678
Filing Date	April 19, 2001
First Named Inventor	Uht, Augustus K.
Art Unit	2183
Examiner Name	O'BRIEN, BARRY J.
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	93	Wallace et al., "Threaded Multiple Path Execution," in *25th Annual International Symposium on Computer Architecture:* ACM, June 1998, pp. 238-249.	
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